REMARKS

Present Status of the Application

Claims 6-13 and 18-25 are pending of which claims 18-25 have been added to more explicitly describe the claimed invention. New claim 18 is fully supported at paragraphs [0003]-[0004] and [0025]. Therefore, it is believed that no new matter adds by way of amendment to claims or otherwise to the application.

Applicants respectfully submit that at least for the following reasons claims 6-13 and 18-25 patently define over prior arts of record. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 102

The Office Action rejected claim 6-13 under 35 U.S.C. 102(b) as being anticipated by Cheng et al. (US-6,353,999, hereinafter Cheng).

Applicants respectfully disagree and submit that it is well established that rejections under 35 U.S.C. 102 requires that each and every elements of the rejected claim must be disclosed exactly by a single prior art reference.

The present invention is generally related to a process for forming a semiconductor packaging substrate. Particularly, claim 6 recites, among other things, [*forming a laminated circuit* having a first surface and a second surface opposite to the first surface, wherein the laminated circuit has a plurality of patterned internal metal layers stacked up, and has a plurality of internal insulation layers each of which is interposed between two adjacent internal metal

layers; and forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit]. The advantage of the above features is that at least the advantages of low cost, high density and high yield of the laminated circuit in the manufacture of the semiconductor packaging substrate can be achieved by integrating the lamination process together with the build-up process.

Applicants respectfully submit that the independent claim 6 is allowable over Cheng because Cheng substantially fails to teach or disclose each and every elements of the claimed invention as claimed in claim 6. More specifically, Cheng fails to teach or disclose a semiconductor packaging substrate comprising at least a laminated circuit; and forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit as required by the proposed independent claim 6.

Instead Cheng, at FIG 6, col. 3, line 39 to col. 4, line 17, substantially teaches a conventional process for manufacturing a semiconductor packaging substrate including forming a multi-layer printed circuit board 216 by alternately stacking a plurality of patterned conductive layers 202b, 202c, 202d, 202e and a plurality of insulation layers 200. Next, through hole is formed in the Multi-layer printed circuit board 216 by a mechanical drilling process. A conductive layer 204 is formed on a sidewall of the through hole, so that the conductive layers 202c, 202d are coupled with each other by the conductive layer 204. Next, insulation layers 214 such as epoxy are formed over both sides of the multi-layer printed circuit board 216 and the through hole is also filled. Conductive layers are formed on the insulation layers 214 by compression, and then the conductive layers are patterned to form conducting wires 202a and

202f. Openings 210 and 212 may be formed in the insulation layers 214 depending on an actual need, and conductive layers 218 are formed in the openings 210 and 212. As a result, the conductive wires 202a and 202f are electrically coupled with the conductive layers 202b and 202e, respectively. In other words, Cheng substantially teaches a conventional process for forming the internal conducting wires/layers and then forming openings to electrically connect the conductive wires with the upper and lower conductive layers (202b, 202e).

Thus, Cheng substantially fails to teach or disclose a process of manufacturing a semiconductor packaging substrate including a lamination process for forming a laminated circuit; and a build-up process for forming external insulation layers and metal layers over the first surface and the second surface of the laminated circuit as required by the claimed invention as claimed in the proposed independent claim 6. In other words, the claimed invention uses the well known lamination process and the well known build-up process to manufacture a semiconductor packaging substrate to gain the advantage of comparatively lower cost lamination process to effectively reduce the manufacturing cost. The lamination process is a well known comparatively lower cost process where a bonding sheet is interposed between the two sheets having a patterned conductive layers formed thereon, thermal compression is carried out to adhere the two sheets, and at least one contact via is formed through the two sheets and the bonding sheet to electrically connect the patterned conductive layers formed on the two sheets with each other. Instead Cheng substantially teaches a process for forming the internal conducting wires and then forming openings to electrically connect the conductive wires/layers with the upper and lower conductive layers (202b, 202e), which is different from that of the

claimed invention. Therefore, Cheng cannot possibly anticipate the proposed independent claim 6 in this regard.

Because the newly added proposed independent claim 18 also recites features that are similar to those of the proposed independent claim 6, therefore Applicants similarly submit that claim 18 also patently defines over Cheng for at least the same reasons discussed above.

Claims 7-13 and 19-25, which directly or indirectly depend from independent Claims 6 and 18, respectively, are also patentable over Cheng at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 6-13 and 18-25 patently define over Cheng. Reconsideration and withdrawal of above rejections is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 6-13 and 18-25 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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